

## ABSTRACT OF THE DISCLOSURE

A high-level synthesis method of the present invention includes:  
generating a CDFG (Control Data Flow Graph) based on an input file describing  
a behavior of a digital circuit; allocating each node of the CDFG generated in  
5 the CDFG generation, expressing contents of processing, to a time  
synchronized with a clock called a Step, based on the CDFG and a constraint  
condition of the digital circuit described in a constraint file, thereby  
scheduling the CDFG; generating allocation information representing how  
resources for constituting the digital circuit are allocated to respective nodes  
10 of the CDFG scheduled in the scheduling, based on resource-level layout  
information representing a layout of the resources, and circuit information  
representing a connecting relationship between the resources; and outputting  
the circuit information generated in the allocation and circuit information  
generation.